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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,307	03/07/2002	Yuji Kawasaki	740756-2446	9633

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EXAMINER	
NGUYEN, JIMMY H	

ART UNIT	PAPER NUMBER
2673	6

DATE MAILED: 01/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,307	KAWASAKI ET AL.	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 July 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/447,932.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is made in response to applicants' preliminary amendment filed on 07/25/2003. Claims 1-23 are currently pending in the application. An action follows below:

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 03/07/2002 and 07/09/2003 and respectively entered as paper No. 2 and 4 are considered by the examiner.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features, "an output of the vertical synchronizing signal" of claims 1 and 5, "an output of the horizontal and vertical synchronizing signals" of claims 3 and 7, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 1, 5, 9, 20 and 23 are objected to because of the following informalities: line 8, "signals", of claim 1, line 8, claim 5, line 8, claim 9, line 7, claim 20, line 7, and claim 23, line 7 should be changed to --signal--, so as to make the invention of claim 1 consistent with the disclosure, i.e., only a single vertical synchronizing signal and a single horizontal synchronizing signal. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-16 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding to claims 1-16, the disclosure, when filed, does not contain sufficient information regarding to the claimed features, "supplying horizontal and vertical signals **to a controller** from **a synchronizing signal generator circuit** ...; and halting **an output of the vertical synchronizing signal from the synchronizing signal generator circuit** ... with each other", as recited in independent **claim 1**, see the last 6 lines, "supplying horizontal and vertical signals **to a controller from a synchronizing signal generator circuit** ...; and halting **an output of the horizontal and vertical synchronizing signals from the synchronizing signal generator circuit** ... with each other", as recited in independent **claim 3**, see the last 6 lines, "supplying horizontal and vertical signals **to a peripheral circuit from a synchronizing signal generator** ...; and halting **an output of the vertical synchronizing signal from the synchronizing signal generator circuit** ... with each other", as recited in independent **claim 5**, see the last 6 lines, "supplying horizontal and vertical signals **to a peripheral circuit from a synchronizing signal generator** ...; and halting **an output of the horizontal and vertical**

synchronizing signal from the synchronizing signal generator circuit ... with each other", as recited in independent **claim 7**, see the last 6 lines, "supplying horizontal and vertical signals **to a display portion** ...; and halting **the supplying of the vertical synchronizing signal to the display portion** ... with each other", as recited in independent **claim 9**, see the last 4 lines, "supplying horizontal and vertical signals **to a display portion** ...; and halting **the supplying of the horizontal and vertical synchronizing signal to the display portion** ... with each other", as recited in independent **claim 13**, see the last 5 lines. The disclosure, specifically fig. 1, page 2, lines 4-11, and page 3, lines 8-12, expressly discloses that a synchronizing signal **generator** circuit 109 for generating synchronizing signals (vertical and horizontal synchronizing signals), and a synchronizing signal **regulating** circuit 108 for regulating vertical and horizontal synchronizing signals and for supplying the **regulated** vertical and horizontal synchronizing signals to the LCD controller 107. However, the disclosure does not contain such description and details the horizontal and vertical synchronizing signals from the synchronizing signal **generator** circuit 109 are supplied to a controller 107, as recited independent claims 1 and 3, or to a peripheral circuit, as recited independent claims 5 and 7, or to a display portion 110, as recited independent claims 9 and 13. Further, the disclosure does not contain such description and details either the vertical synchronizing signal or the horizontal synchronizing signal comprising an output, in the manner as recited in claims 1, 3, 5 and 7. Accordingly, the disclosure, when filed, does not contain such description and details regarding to the above underlined features, so as to enable one skilled in the pertinent art to make and use the claimed invention.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-11, 13-15 and 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuki et al. (USPN: 5,374,941, cited in IDS No. 2), hereinafter Yuki, and further in view of Nishikawa (JP 04-050996 A, cited in IDS No. 4).

As per claims above, Yuki discloses a liquid crystal display (LCD) device and an associate method of driving the LCD device, the device comprising a simple matrix LCD display portion (1) (fig. 1B, col. 2, lines 63-64), a VRAM 7 for storing a first image data (fig. 1A, col. 5, lines 19-22), a VRAM 8 for storing a second image data (fig. 1A, col. 5, lines 19-22), a comparator circuit (11) (fig. 1A, col. 5, lines 22-27), a synchronizing signal generator circuit (a graphic card, fig. 1A) for outputting a horizontal synchronizing signal (HSYNC) and a vertical synchronizing signal (VSYNC), and a controller (a circuit including elements 12-15 and 5, figs. 1A-1B). Accordingly, Yuki discloses all the claimed limitations of these claims except for a synchronizing signal regulator circuit for supplying the regulated synchronizing signals to a controller if the first image data and the second image data are different from each other and for halting the regulated synchronizing signals to a controller if the first image data and the second image data coincide with each other, as recited in these claims.

However, Nishikawa discloses a related LCD device (see fig. 1) comprising a synchronizing signal regulator circuit (a circuit comprising two AND gates 107 and 108, fig. 1)

for receiving a horizontal synchronizing signal (HSYNC), a vertical synchronizing signal (VSYNC) and a standby signal (STNBY), for supplying a regulated horizontal synchronizing signal (an output of an AND gate 108, fig. 1) and a regulated vertical synchronizing signal (an output of an AND gate 107, fig. 1) to a controller (a circuit including elements as shown in fig. 1 except for elements 107 and 108), and for halting the regulated horizontal and vertical synchronizing signals to a controller when the display device is in a standby state (by virtue of the function of the two AND gates 107 and 108), see abstract. Further, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to recognize that when the display device is in a standby state, the two frame image data coincide with each other. In other words, Nishikawa obviously teaches the synchronizing signal regulator circuit (107, 108) for halting the regulated synchronizing signals to a controller if the first image data and the second image data coincide with each other. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the synchronizing signal regulator circuit in the Yuki display device, in view of the teaching in the Nishikawa reference, because this would reduce the electric power consumption, as taught by Nishikawa (see abstract).

9. Claims 1-10, 12-14 and 16-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (USPN: 5,434,589), hereinafter Nakamura, and further in view of Nishikawa.

As per claims above, Nakamura discloses a liquid crystal display (LCD) device and an associate method of driving the LCD device, the display device (see fig. 2) comprising an active

matrix LCD display portion (37), a VRAM for storing a first image data and a second image data (col. 2, lines 21-26), and a display controller 24. As noting in fig. 5 and at col. 2, lines 35-42, and col. 7, lines 35-46, Nakamura further teaches a LCD device comprising a comparator circuit (a coincidence detector including element 71, 69 and 73) for comparing the first and second image data to detect whether the first and second image data coincide with each other. Accordingly, Nakamura discloses all the claimed limitations of these claims except for a synchronizing signal regulator circuit for supplying the regulated synchronizing signals to a controller if the first image data and the second image data are different from each other and for halting the regulated synchronizing signals to a controller if the first image data and the second image data coincide with each other, as recited in these claims.

However, Nishikawa discloses a related LCD device (see fig. 1) comprising a synchronizing signal regulator circuit (a circuit comprising two AND gates 107 and 108, fig. 1) for receiving a horizontal synchronizing signal (HSYNC), a vertical synchronizing signal (VSYNC) and a standby signal (STNBY), for supplying a regulated horizontal synchronizing signal (an output of an AND gate 108, fig. 1) and a regulated vertical synchronizing signal (an output of an AND gate 107, fig. 1) to a controller (a circuit including elements as shown in fig. 1 except for elements 107 and 108), and for halting the regulated horizontal and vertical synchronizing signals to a controller when the display device is in a standby state (by virtue of the function of the two AND gates 107 and 108), see abstract. Further, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to recognize that when the display device is in a standby state, the two frame image data coincide with each

other. In other words, Nishikawa obviously teaches the synchronizing signal regulator circuit (107, 108) for halting the regulated synchronizing signals to a controller if the first image data and the second image data coincide with each other. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the synchronizing signal regulator circuit in the Nakamura display device, in view of the teaching in the Nishikawa reference, because this would reduce the electric power consumption, as taught by Nishikawa (see abstract).

Double Patenting

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 17, 18, 20, 21 and 23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2 and 19 of U.S. Patent No. 5,812,149 cited in IDS No. 2. Although the conflicting claims are not identical, they are not patentably distinct from each other because the subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: a display portion, at least one VRAM,

comparing means, output means, control means, a timer, a backlight unit and a synchronizing signal generating means along with the interconnections between them.

12. Claims 1-16, 19 and 22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 5,812,149 in view of Nishikawa.

As per claims above, claim 2 of U.S. Patent No. 5,812,149 discloses a LCD device comprising a display portion, memory means including a VRAM, a comparator (comparing means), a synchronizing signal regulator circuit (output means) and a controller (control means). Accordingly, claim 2 of U.S. Patent No. 5,812,149 discloses all the claimed limitations except for a synchronizing signal regulator circuit for halting the regulated synchronizing signals to a controller if the first image data and the second image data coincide with each other.

However, Nishikawa discloses a related LCD device (see fig. 1) comprising a synchronizing signal regulator circuit (a circuit comprising two AND gates 107 and 108, fig. 1) for receiving a horizontal synchronizing signal (HSYNC), a vertical synchronizing signal (VSYNC) and a standby signal (STNBY), for supplying a regulated horizontal synchronizing signal (an output of an AND gate 108, fig. 1) and a regulated vertical synchronizing signal (an output of an AND gate 107, fig. 1) to a controller (a circuit including elements as shown in fig. 1 except for elements 107 and 108), and for halting the regulated horizontal and vertical synchronizing signals to a controller when the display device is in a standby state (by virtue of the function of the two AND gates 107 and 108), see abstract. Further, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to recognize

that when the display device is in a standby state, the two frame image data coincide with each other. In other words, Nishikawa obviously teaches the synchronizing signal regulator circuit (107, 108) for halting the regulated synchronizing signals to a controller if the first image data and the second image data coincide with each other. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to modify the synchronizing signal regulator circuit of the invention defined in claim 2 of U.S. Patent No. 5,812,149 to also provide a capability of halting the regulated synchronizing signals to a controller if the first image data and the second image data coincide with each other, in view of the teaching in the Nishikawa reference, because this would reduce the electric power consumption, as taught by Nishikawa (see abstract).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is (703) 306-5422. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at (703) 305-4938.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)